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Customer No.: 31561
Docket No.: 12008-US-PA
Application No.: 10/709,824

AMENDMENT

To the Claims:

Claim 1. (original) A frequency synthesizing and back-end processing circuit, comprising:

a frequency synthesizer, operated by a clock signal, said frequency synthesizer including

a first multiplexer;

a first memory unit, coupled to said first multiplexer, for storing a first reference frequency;

a second memory unit, coupled to said first multiplexer, for storing a second reference frequency;

a shift register, for storing a target frequency and comparing the target frequency with a predetermined value;

a control unit, coupled to said shift register, said control unit based on a result of comparing said target frequency with said predetermined value selecting one of said first reference frequency and said second reference frequency passes said first multiplexer;

a digital-to-analog converter, for converting a first signal passing through said first multiplexer to a second signal; and

a second multiplexer, based on a control signal passing one of said first signal and said second signal to obtain a third signal; and

a back-end processing circuit, including

a mixer, coupled to said second multiplexer for receiving said third signal; and

a filter, coupled to said mixer.

Claim. 2 (original) The circuit of claim 1, wherein said shift register is a linear feedback shift register.

Claim 3. (original) The circuit of claim 2, wherein said result of comparing said target frequency with said predetermined value determines one of said first reference frequency and said second reference frequency passes said first multiplexer, said target frequency then shifts one bit responsive to said clock signal for comparing with said predetermined value again until a frequency resolution cannot distinguish a difference between said target frequency and said predetermined value.

Claim 4. (original) The circuit of claim 2, wherein the number of stages of said linear feedback shift register determines said frequency resolution, said frequency resolution is a ratio of a difference between said first frequency and said second frequency to a base 2 multiple exponential, said multiple is a number of said stages of said linear feedback shift register.

Claim 5. (original) The circuit of claim 1, wherein when said control signal selects said first signal to pass through said second multiplexer, said mixer mixes said third signal and a signal generated by a numerical controlled oscillator.

Claim 6. (original) The circuit of claim 1, wherein when said control signal selects said second signal to pass through said second multiplexer, said mixer mixes said third signal and a signal generated by a voltage controlled oscillator.

Claim 7. (original) The circuit of claim 1, wherein said filter is a low pass filter.

Claim 8. (original) The circuit of claim 1, wherein said filter is a band pass filter.

Claim 9. (original) The circuit of claim 1, wherein said filter is a high pass filter.

Claims 10. (currently amended) A method for frequency synthesizing and back-end processing, comprising:

~~a frequency synthesizing method, including applying interpolation to synthesize a synthesized frequency satisfying a predetermined resolution~~

comparing a target frequency with a predetermined value to obtain a comparing result;

selecting one of a first reference frequency and a second reference frequency according to the comparing result to generate a digital signal having a selected reference frequency;

converting the digital signal having the selected reference frequency into an analog signal;

selecting one of the digital signal and the analog signal;

~~a back-end processing method, including a mixing method and a filtering method~~

mixing a signal selected from the digital signal and the analog signal to obtain a mixed signal; and

filtering said mixed signal.

Claim 11. (cancelled)

Claim 12. (currently amended) The method of claim 10, wherein the step of ~~said~~ mixing ~~method includes~~ a signal selected from the digital signal and the analog signal comprises:

if the digital signal is selected, then mixing the digital signal with a signal generated by a numerical controlled oscillator.

Claim 13. (currently amended) The method of claim 10, wherein the step of ~~said~~ mixing ~~method includes~~ a signal selected from the digital signal and the analog signal comprises:

if the analog signal is selected, then mixing the analog signal with a signal generated by a voltage controlled oscillator.

Claim 14. (currently amended) The method of claim 10, wherein the step of filtering said mixed signal ~~said filtering method includes~~ comprises:

performing a low pass filtering operation on said mixed signal~~method~~.

Claim 15. (currently amended) The method of claim 10, wherein the step of filtering said mixed signal ~~said filtering method includes~~ comprises:

performing a band pass filtering operation on said mixed signal~~method~~.

Claim 16. (currently amended) The method of claim 10, wherein the step of filtering said mixed signal ~~said filtering method includes~~ comprises:

performing a high pass filtering operation on said mixed signal~~method~~.

Claim 17 (new) A frequency synthesizer, comprising:

a first multiplexer;

a first memory unit, coupled to said first multiplexer, for storing a first reference frequency;

a second memory unit, coupled to said first multiplexer, for storing a second reference frequency;

a shift register, for storing a target frequency and comparing the target frequency with a predetermined value; and

a control unit, coupled to said shift register, said control unit based on a result of comparing said target frequency with said predetermined value selecting one of said first reference frequency and said second reference frequency passes said first multiplexer.

Claim 18 (new) The frequency synthesizer of claim 17, wherein said shift register is a linear feedback shift register.

Claim 19 (new) The frequency synthesizer of claim 18, wherein said result of comparing said target frequency with said predetermined value determines one of said first reference frequency and said second reference frequency passes said first multiplexer, and said target frequency then shifts one bit responsive to said clock signal for comparing with said predetermined value again until a frequency resolution cannot distinguish a difference between said target frequency and said predetermined value.

Claim 20 (new) The frequency synthesizer of claim 18, wherein the number of stages of said linear feedback shift register determines said frequency resolution, said frequency resolution is a ratio of a difference between said first frequency and said second frequency to a base 2 multiple exponential, and said multiple is a number of said stages of said linear feedback shift register.